

A. Remarks

Applicants respectfully request that the rejections of record be reconsidered in light of their remarks set forth below, and that the subject application be passed to issuance in view thereof.

In the Office Action, claims 1, 24-28, and 30 stand rejected as being anticipated by the Sano et al patent, USP 6,040,605 (hereafter "Sano"). In response, Applicants respectfully submit that Sano neither teaches nor suggests the invention as set forth in the rejected claims. With reference to claim 1, note that the invention is recited as including the step of "removing" the base layer from which the epitaxial channel is formed. As shown in Figs. 1(b) and 16(b) of Sano, the silicon layers 76, 77 remain in place after the channel silicon 78 is formed - none of these layers are etched after the channel region is formed, let alone "removed" as recited. As a result, in Sano the "second sidewall" of the epi channel is not exposed, as recited in claim 1 - rather, the second sidewall of the channel region 78 remains covered by the silicon layers 76, 77. In combination, these steps as recited in claim 1 result in the formation of a freestanding epi channel, as shown in Fig. 6, which is neither shown nor suggested by Sano. Applicants respectfully submit that these claimed features patentably distinguish from Sano, and as such the rejection of record as to claim 1 has been traversed.

Turning to claim 24, the invention is recited as including the step of "forming a first semiconductor layer having first and second ends and a central region that is thinner than said first and second ends, said central region having first and second side surfaces." There is no semiconductor layer in Sano that includes these features. The semiconductor layers in Sano are layers 86, 76, 77, and 78. None of these layers have any features remotely resembling "...a central region that is thinner than the first and second ends," wherein the epitaxial channel regions are formed on side surfaces of this central region, as recited. Applicants respectfully submit that these claimed features patentably distinguish from Sano, and as such the rejection of record as to claim 24 (as well as its dependent claims 25-28 and 30) has been traversed.

In the Office Action, claims 14-19 and 22-23 stand rejected under 35 USC 102 in view of the

Neudeck et al patent (USP 5,273,921, "Neudeck"). In response, Applicants respectfully submit that Neudeck neither teaches nor suggests the invention as set forth in the claims set forth above.

In general, with reference to Fig. 1H, Neudeck teaches a double gate FET in which the channel region 18 sits atop a first gate electrode 14 and below a second gate electrode 20. Channel region 18 is epitaxially grown from an underlying silicon source 11. Source and drain regions 31, 32 are epitaxially grown from the channel region 18, and apparently are implanted to form LDD structures 31A, 32A adjacent the channel region.

With reference first to rejected claim 14, note that the claim specifies the formation of first and second epitaxially-grown channel regions, and that the gate contacts side surfaces and a top surface of the channel region. As pointed out in response to the previous office action, Neudeck does not show plural channels as recited, only one. Moreover, in claim 14 the source and drain regions are recited as being etched from a silicon layer, such that they contact respective ones of the two channels. In Neudeck the source and drains are epitaxially grown; there is no etch process taught in connection with forming the source and drain regions, as recited. Finally, the gate electrodes 14, 20 of Neudeck do not contact a top surface and first and second side surfaces of the channel region, as recited. The gate 14 is below the channel 18, and the gate 20 is above it. These are not "side surfaces" of anything. Even if we were to read "side surfaces" as the lower and upper surfaces of the channel 18, note there is no gate that abuts what would have to be interpreted as a "top surface" - the sides of channel 18 where the source/drain regions are grown. Applicants respectfully submit that these claimed features patentably distinguish from Neudeck, and as such the rejection of record as to claim 14 (as well as its rejected dependent claims 15-19 and 22-23) has been traversed.

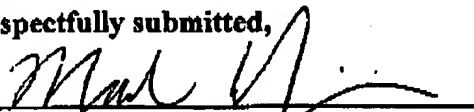
With reference to claim 15, in addition to incorporating the aforementioned distinguishing features of claim 14 from which it depends, note that claim 15 recites the creation of silicon lines that contact the source/drain regions, on which etch stop layers are formed, and on which the epi channels are formed, the lines and the etch stops being subsequently removed. Neudeck neither teaches nor suggests this combination of steps. In Neudeck there are no semiconductor "lines"

that contact the source/drain regions as recited (rather, the source/drain regions 31, 32 are insulated from the other semiconductor layers, they are not in contact with any other semiconductor); there is no etch stop layer grown on a "side surface" of a "line" as recited (the etch stop 16 is formed on an upper surface of an oxide 12, not on a "side surface" of anything, let alone a "semiconductor line"); and there is no operation shown in which the recited line, along with the etch stop, is removed as recited. Applicants respectfully submit that these claimed features patentably distinguish from Neudeck, and as such the rejection of record as to claim 15 has been traversed.

In the Office Action claims 20, 21, and 29 stand objected to as depending on rejected base claims, and are indicated as being allowable if rewritten in independent form. In response, Applicants submit that for the foregoing reasons, the base claims on which these claims depend are patentable over the art of record. Accordingly, Applicants respectfully submit that the objections of record to claims 20, 21, and 29 have been traversed.

In view of the foregoing, applicants respectfully submit that all of claims 1 and 14-30 as submitted herein recite patentable subject matter, and accordingly they earnestly solicit passage of the subject US patent application to issuance in view thereof. Should the examiner have any comments, questions, or suggestions, he is urged to contact the undersigned attorney at the telephone number or email listed below.

Respectfully submitted,



Mark F. Chadurjian
Registration Number 36,739
802 769-8843

IBM Intellectual Property Law 972E
1000 River Street
Essex Junction VT, 05452